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JC713 U.S. PTO 12/28/99

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 42390.P7663 Total Pages 2

First Named Inventor or Application Identifier Kristopher Frutschy

Express Mail Label No. EL414970448US

JC542 U.S. PTO 09/473305 12/28/99

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 24)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 11)

4. X Oath or Declaration (Total Pages 4 (unsigned))

a. ___ Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. _ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. _ Microfiche Computer Program (Appendix)

7. __ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. __ Assignment Papers (cover sheet & documents(s))
9. __ a. 37 CFR 3.73(b) Statement (where there is an assignee)
__ b. Power of Attorney
10. __ English Translation Document (if applicable)
11. __ a. Information Disclosure Statement (IDS)/PTO-1449
__ b. Copies of IDS Citations
12. __ Preliminary Amendment
13. X Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. __ a. Small Entity Statement(s)
b. Statement filed in prior application, Status still proper and desired
15. __ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. __ Other: _____

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:
____ Continuation ____ Divisional ____ Continuation-in-part (CIP)
of prior application No: _____

18. **Correspondence Address**
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PATENT
Ref. No. P7663

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APPLICATION FOR UNITED STATES PATENT

FOR

DIRECT BGA ATTACHMENT WITHOUT SOLDER REFLOW

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DIRECT BGA ATTACHMENT WITHOUT SOLDER REFLOW

BACKGROUND OF THE INVENTION

Field of the Invention: The present invention relates to apparatus and processes for packaging microelectronic device. In particular, the present invention relates to a packaging technology that utilizes compression for achieving a BGA surface mount-type electrical connection between a microelectronic device and a carrier substrate.

State of the Art: A variety of techniques are known in the art for attaching microelectronic devices (such as microprocessors, circuit components, and the like) to carrier substrates (such as motherboards, expansion cards, and the like). These techniques may include direct surface mounting of the microelectronic device to the carrier substrate and socket mounting of the microelectronic device. Socket mounting may comprise a socket mounted on the carrier substrate wherein the microelectronic device is attached to the socket by pins protruding from the microelectronic device, or wherein the microelectronic device is pressed into the socket to achieve electrical continuity between a plurality of lands on the microelectronic device and a plurality of terminals on the socket. However, in low profile applications, such as laptop computers, the height of the attachment of the microelectronic device must be minimized. Thus, sockets are usually not utilized because the socket adds an unacceptable amount of height to the assembly. Thus, for low profile applications, direct surface mounting is generally used.

FIG. 5 illustrates an exemplary surface mounted land grid array 200 comprising a microelectronic device package 208 including a microelectronic device 202 attached to

and in electrical contact with a first surface 206 of an interposer substrate 204. The attachment and electrical contact may be achieved through a plurality of small solder balls 212 extending between contacts 214 on the microelectronic device 202 and contacts 216 on the interposer substrate first surface 206. An underfill material 218 may be disposed between the microelectronic device 202 and the interposer substrate 204 to prevent contamination. Further, a thermal interface (shown as heat slug 222) for dissipation of heat generated by the microelectronic device 202 during operation may be attached thereto. The interposer substrate first surface contacts 216 are in discrete electrical contact with contacts 224 on a second surface 226 of the interposer substrate 204 through a plurality of conductive traces (not shown) extending through the interposer substrate 204.

The electrical contact of the microelectronic package 208 to a carrier substrate (such as a motherboard) 232 is achieved with a plurality of solder balls 234 which extend discretely between the interposer substrate second surface contacts 224 and contacts 236 on a first surface 238 of the carrier substrate 232. The solder balls 234 are reflowed (i.e., melted) which attaches the interposer substrate 204 to the carrier substrate 232. This form of electrical attachment is called a ball grid array ("BGA") attachment. The carrier substrate 232 includes conductive traces therein and/or thereon (not shown) which form electrical pathways to connection the first surface contacts 236 with external components (not shown).

The microelectronic device 202 and the interposer substrate 204 may be supported by a support structure 242. The support structure 242 includes a frame 244, a

backing plate 246, a thermal plate 248, and a plurality of retention devices (shown as bolts 252 and nuts 254). The backing plate 246 is placed adjacent a second surface 256 of the carrier substrate 232. The frame 244 is placed adjacent to the carrier substrate first surface 238 and at least partially surrounds the microelectronic package 208. The thermal plate 248 abuts the heat slug 222 and extends over the frame 244. The bolts 252 extend through the backing plate 246, the frame 244, and the thermal plate 248, and are retained by nuts 254 threaded thereon. The frame 244 not only acts to support the assembly, but also acts as a stop to prevent overtightening of the retention devices, which could damage the microelectronic device. The thermal plate 248 is generally thermally conductive to assist the heat slug 222 in removing heat generated by the operation of microelectronic device 202.

Although the surface mounted land grid array 200 shown in FIG. 4 achieves a low profile, the attachment of the microelectronic device package 208 to the carrier substrate 232 by reflowing of the solder balls 234 makes it difficult to remove the microelectronic device package 208 after attachment. This, in turn, makes it difficult to replace a defective microelectronic device (resulting in high rework costs) and makes it difficult for an end user or retailer to upgrade the microelectronic device.

Therefore, it would be advantageous to develop new apparatus and techniques to provide a low profile microelectronic device attachment which allows for easy removal of the microelectronic device.

SUMMARY OF THE INVENTION

The present invention relates to a packaging technology that achieves a BGA surface mount-type electrical connection between a first substrate and a second substrate by pressure on the BGA solder balls rather than by the reflow thereof. An embodiment of the present invention includes a microelectronic component assembly comprising a first substrate having at least one contact and a second substrate having at least one contact. At least one solder ball extends between the first substrate contact and the second substrate contact, wherein the solder ball is attached to the first substrate contact. A compression mechanism imparts pressure between the first substrate and the second substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

FIG. 1 is a side cross-sectional view of an embodiment of a microelectronic device assembly, according to the present invention;

FIGs. 2a-2g are side cross-sectional views of alternate embodiments of contact configurations, according to the present invention;

FIG. 3 is a side cross-sectional view of another embodiment of a microelectronic device assembly, according to the present invention;

FIG. 4 is a flow chart illustrating a process for forming a microelectronic device assembly, according to the present invention; and

FIG. 5 is a cross-sectional view of a microelectronic device assembly, as known in the art.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENT

Although FIGs. 1, 2a-2g, and 3 illustrate various views of the present invention, these figures are not meant to portray microelectronic assemblies in precise detail. Rather, these figures illustrate microelectronic assemblies in a manner to more clearly convey the concepts of the present invention. Additionally, elements common between the figures retain the same numeric designation. Further, it is noted that the term "substrate", as used in the present application, includes but is not limited to carrier substrates, interposer substrates, microelectronic devices (semiconductor chips and the like), and combinations of interposer substrates and microelectronic devices.

This present invention provides a surface mount-type microelectronic component assembly which does not physically attach the microelectronic component to its carrier substrate. Electrical contact is achieved between the microelectronic component and the carrier with solder balls attached to either the microelectronic component or the carrier substrate. A force is exerted on the assembly to achieve sufficient electrical contact between the microelectronic component and the carrier substrate. Thus, the present invention has advantages of a surface mounted assembly (low mounted height and low inductance due to a short electrical path between microelectronic component and carrier

substrate), while also having the advantages of a socket-type assembly (easy removal and/or replacement of the microelectronic component).

FIG. 1 illustrates a microelectronic component assembly 100 according to one embodiment of the present invention. The microelectronic component assembly 100 includes a microelectronic device package 108 comprising a microelectronic device 102 attached to and in electrical contact with a first surface 106 of an interposer substrate 104. The attachment and electrical contact is achieved through a plurality of small solder balls 112 extending between contacts 114 on the microelectronic device 102 and contacts 116 on the interposer substrate first surface 106. It is, of course, understood that the microelectronic device 102 could be electrically attached to the interposer substrate 104 with a variety of techniques, including but not limited to conductive epoxy interconnects, lead finger connections, TAB connection, wire bonds, etc. An underfill material 118 may be disposed between the microelectronic device 102 and the interposer substrate 104 to prevent contamination. Further, a thermal interface (shown as heat slug 122) for dissipation of heat generated by the microelectronic device 102 during operation may be attached thereto. The interposer substrate first surface contacts 116 are in discrete electrical contact with contacts 124 on a second surface 126 of the interposer substrate 104 through a plurality of conductive traces (not shown) extending through the interposer substrate 104.

The electrical contact of the microelectronic package 108 with a carrier substrate (such as a motherboard) 132 is achieved with a plurality of solder balls 134, which are formed (reflow) on the interposer substrate second surface contacts 124. The solder

balls 134 extend discretely between the interposer substrate second surface contacts 124 and contacts 136 on a first surface 138 of the carrier substrate 132. The solder balls 134 are not physically attached to the carrier substrate contacts 136. Rather, the solder balls 134 make electrical contact by being pressed onto the carrier substrate contacts 136 by a support structure 142. The support structure 142 also holds the microelectronic device 102 and the interposer substrate 104 in place. The solder balls 134 and the carrier substrate contacts 136 may be formed from any applicable conductive material and may include, but is not limited to lead, tin, indium, gallium, bismuth, cadmium, zinc, copper, gold, silver, antimony, germanium, and alloys thereof. As contact resistance is a factor in the present invention, it is preferred that the solder balls 134 and the carrier substrate contacts be made of gold or plated with gold. With regard to the solder balls 134, at least a portion of the solder ball 134 which will contact the carrier substrate contacts 136 is preferably plated with gold. Of course, the gold plating must be sufficiently thick so that the gold does not completely diffuse into the solder ball 134 or into the carrier substrate contact 136 during the lifetime of the microelectronic component assembly 100.

The support structure 142 includes a frame 144, a backing plate 146, a thermal plate 148, and a plurality of retention devices (shown as bolts 152 and nuts 154). The backing plate 146 is placed adjacent a second surface 156 of the carrier substrate 132. The frame 144 is placed adjacent to the carrier substrate first surface 138 and at least partially surrounds the microelectronic device package 108. The frame 144 is preferably designed to reside close to the interposer substrate 104 (i.e., minimum

clearance between the frame 144 and the interposer substrate 104). The minimum clearance allows the frame 144 to align the solder balls 134 with their respective carrier substrate contacts 136. Furthermore, the frame 144 will act as a stop tp prevent overtightening of the support structure 142.

The thermal plate 148 abuts the heat slug 122 and extends over the frame 144. The bolts 152 extend through the backing plate 146, the frame 144, and the thermal plate 148, and are retained by nuts 154 threaded thereon. The thermal plate 148, the frame 144, and backing plate 146 are preferably made of substantially rigid material, such as metal (e.g., aluminum), so that each are rigid enough not to flex or deform under pressure (approximately 22.68 kgf (50 lbf) or greater), as discussed below.

The thermal plate 148 is preferably thermally conductive to assist the heat slug 122 in removing heat generated by the operation of microelectronic device 102. It is, of course, understood that the heat slug 122 may not be necessary, as the thermal plate 148 may directly abut the microelectronic device 102 to dissipate the heat generated therefrom.

The support structure 142 further includes a resilient spacer 158 disposed between the interposer substrate first surface 106 and the thermal plate 148. The resilient spacer 158 is used to more evenly distribute pressure imposed by the support structure 142 across the interposer substrate 104. The resilient spacer 158 may be made of any appropriate resilient material, including but not limited to rubber, foam, elastomer, polymer materials, and the like. The support structure 142 is, thus, a compression mechanism for imparting pressure between the interposer substrate 104 and the carrier

substrate 132. The pressure imposed on the resilient spacer 158 and the thermal interface is regulated by tightening or loosening the nuts 154 on the bolts 152, subject to a height of the frame 144 and the resilience of the resilient spacer 158. The pressure imposed on the resilient spacer 158 and the thermal interface presses the solder balls 134 against the carrier substrate contacts 136, which allows the solder balls 134 to achieve sufficient electrical contact with the carrier substrate contacts 136 without having to reflow the solder balls 134.

The carrier substrate contacts 136 may have a variety of configurations. FIGs. 2a-2e are enlargements of inset 2 of FIG. 1 and illustrate a few of such configurations. As shown in FIG. 2a, carrier substrate contacts 136a may be substantially planar, wherein the solder ball 134 is pressed against a first surface 162 of the planar carrier substrate contact 136a.

Although, the use of a substantially planar carrier substrate contacts 136a, as shown in FIG. 2a, is typical in current carrier substrate designs, a planar carrier substrate contact 136a may not achieve a sufficient electrical contact with the solder ball 134 due to the low surface area of contact therebetween (i.e., the contact resistance is too high). Furthermore, since most ball grid arrays do not have perfectly matched solder ball sizes (i.e., the solder balls are not coplanar across there contact surfaces), smaller solder balls in the grid array are less likely to achieve a sufficient electrical contact. FIGs. 2b-2e illustrate various configurations for the carrier substrate contact which will increase the contact surface area between the solder balls and the carrier

substrate contacts and/or reduce the effects of non-coplanarity, thereby lowering the contact resistance.

As shown in FIG. 2b, a carrier substrate contact 136b may be a narrow recess, wherein the solder ball 134 is pressed against and deformed to contact upper planar surfaces 164 and sidewalls 166 of the narrow recess carrier substrate contact 136b. Such a configuration provides a higher surface area contact of the solder ball 134 to the narrow recess carrier substrate contact 136b than the planar carrier substrate contact 136a of FIG. 2a. Furthermore, this design allows taller/larger solder balls in a non-coplanar array to be compressed farther into the narrow recess carrier substrate contact 136b which allows shorter/smaller solder balls to achieve sufficient electrical contact.

As FIGs. 2c illustrates, wide recess carrier substrate contacts 136c may be fabricated to have substantially vertical sidewalls 166 and having a width 168 which is substantially the same or only slightly smaller than a diameter 172 of the solder balls 134. This contact design allows the solder ball 134 to slide into the wide recess carrier substrate contact 136c. It is preferred the solder ball 134 and/or the sidewalls 166 be deformable to allow the solder ball 134 to easily slide into the wide recess carrier substrate contact 136c. Such a configuration provides a high surface area contact between the solder ball 134 to the sidewalls 166. Furthermore, this design also allows taller/larger solder balls in a non-coplanar array to be extend farther into the wide recess carrier substrate contact 136c which allows shorter/smaller solder balls to achieve sufficient electrical contact.

As shown in FIG. 2d, carrier substrate contacts 136d may be substantially cup-shaped (i.e., semispherical), wherein the solder ball 134 is pressed against a curved surface 178 of the carrier substrate contact 136d residing within a semispherical recess 177 formed in the carrier substrate 132. The curved surface 178 is preferably configured to have a radius that substantially matches the radius of the solder ball 134 (both radii illustrated as element 176). Such a configuration provides high surface area contact of the solder ball 134 with the cup-shaped carrier substrate contact 136d. However, the configuration in FIG. 2d does not compensate for non-coplanarity of the solder balls 134. Thus, FIG. 2e illustrates an embodiment wherein the semispherical recess 177 is formed in the substrate 104 with a carrier substrate contact 136e extending over the semispherical recess 177 to form a void. Thus, the solder 134 and the carrier substrate contact 136e flex into the semispherical recess 177 when pressure is imparted thereon, which compensates for the non-coplanarity of the solder balls 134. FIG. 2f illustrates another embodiment wherein a resilient material layer 179 is disposed between the semispherical recess 177 and the carrier substrate contact 136f, wherein the resilient material layer 179 will flex to compensate for the non-coplanarity of the solder balls 134.

It is, of course, understood that the contact configuration can be reversed. For example, as shown in FIG. 2g, the solder balls 134 may be formed (reflowed) on the contact 136g of the carrier substrate 132, wherein the solder balls 134 are pressed into the interposer substrate second surface contacts 124. It is believe the forming the solder balls 134g on the carrier substrate 132 will result in a higher coplanarity (i.e., even

solder ball height) the forming the solder balls on the interposer substrate 104. Of course, the interposer substrate second surface contacts 124 may also have a variety of configurations, such as illustrated for the carrier substrate contacts 136a-136f (FIGs. 2a-2f, respectively).

It is also understood that the configurations are not limited to the configurations illustrated in FIGs. 2a-2g, but may have any acceptable configuration that can be devised by one skilled in the art.

It is, of course, understood that the present invention is not limited to attachment of an interposer substrate to a carrier substrate. The present invention may also be utilized to directly attach a microelectronic device (also broadly defined as a "substrate") to a carrier substrate. FIG. 3 illustrates such a microelectronic component assembly 180 wherein the microelectronic device 102 is attached to and in electrical contact with the contacts 136 on the first surface 138 of the carrier substrate 132. The attachment and electrical contact is achieved through a plurality of solder balls 134 formed (reflowed) on the microelectronic device contacts 114 which physically contact the carrier substrate contacts 136. A thermal interface (shown as heat slug 122) for dissipation of heat generated by the microelectronic device 102 during operation may be attached to the microelectronic device 102. As with the embodiment illustrated in FIG. 1, the support structure 142 provides the pressure for achieving the electrical contact between the microelectronic device 102 and the carrier substrate 132. However, the resilient spacer 158, as shown in FIG. 1, is not required as the support structure 142 will inherently distribute the pressure substantially evenly across the

microelectronic device 102. It is, of course, understood that either the microelectronic device contacts 114 or the carrier substrate contacts 136 may have a variety of configurations, such as illustrated in FIGs. 2a-2g.

A bench test was run in which an organic land grid array having 615 gold coated solder balls (30 mils in diameter with about 10 microinches of gold plating) was pressed against a test board which had corresponding gold coated planar contacts (about 10 microinches of gold plating). An electrical continuity across the solder ball-to planar contact junctions of about 57% was achieved at about 37, 52, and 67 gramf/solder ball nominal applied force. Of course, the bench test was not optimized. Rather the bench test was run for concept validation only. However, it is believed that an optimized configuration would achieve a solder ball-to-contact resistance below 20 mOhms with an applied force of about 35 gramf/solder ball or greater.

FIG. 4 is a flowchart of a method 180 of fabricating a microelectronic device assembly of the present invention. As described in box 182, the frame is placed on the first surface of the carrier substrate and the backing plate is place on the second surface of the carrier substrate. As described in box 184, bolts are inserted through the backing plate, the carrier substrate and the frame. A substrate (such as a microelectronic device or a microelectronic device attached to an interposer substrate) is then inserted into the frame, as described in box 186, wherein the frame guides the substrate into alignment. This alignment positions the contacts of the substrate to match the location of the contacts on the carrier substrate. Thus, solder balls formed on the substrate contacts come into discrete physical contact with the carrier substrate contracts, or solder balls

formed on the carrier substrate contacts come into discrete physical contact with the substrate contracts.

As described in box 188, a thermal interface is then place on the microelectronic device. Optionally, when the substrate is a microelectronic device attached to an interposer substrate, a resilient spacer is place on the interposer substrate, as described in box 190. A thermal plate is installed on top of the thermal interface and the resilient spacer (if one is used), such that the thermal plate can be retained by the bolts, as described in box 192. As described in box 194, nuts are attached to the bolts and tightened to exert a force on the thermal interface and resilient spacer (if one is used). This force is translated through the assembly to press the solder balls into electrical contact, as previously discussed.

Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A microelectronic component assembly, comprising:

a first substrate having at least one contact;

a second substrate having at least one contact;

at least one solder ball extending between said at least one first substrate contact and said at least one second substrate contact, wherein said at least one solder ball is attached to said at least one first substrate contact; and

a compression mechanism for imparting pressure between said first substrate and said second substrate.

2. The microelectronic component assembly of claim 1, wherein said first substrate comprises a microelectronic device package.

3. The microelectronic component assembly of claim 1, wherein said first substrate comprises a carrier substrate.

4. The microelectronic component assembly of claim 1, wherein said first substrate comprises a microelectronic device.

5. The microelectronic component assembly of claim 1, wherein said at least one second substrate contact comprises a recess defined by at least one sidewall extending into said second substrate.

6. The microelectronic component assembly of claim 5, wherein said at least one recessed second substrate contact includes a width which is substantially the same as a diameter of said solder ball.

7. The microelectronic component assembly of claim 5, wherein said at least one recessed second substrate contact has a semispherical surface which is substantially the same radius as a radius of said solder ball.

8. A method of fabricating a microelectronic component assembly, comprising:

providing a first substrate having at least one contact;

providing a second substrate having at least one contact;

attaching at least one solder ball on said at least one first substrate contact;

aligning said at least one solder ball with said at least one second substrate contact; and

imparting pressure between said first substrate and said second substrate.

9. The method of claim 8, wherein providing said first substrate comprises providing a microelectronic device package.

10. The method of claim 8, wherein providing said first substrate comprises providing a carrier substrate.

11. The method of claim 8, wherein providing said first substrate comprises providing a microelectronic device.

12. A microelectronic component assembly, comprising:

a first substrate having a first surface and a second surface, wherein said first substrate first surface includes at least one contact;

a second substrate having a first surface and a second surface; wherein said second substrate first surface includes at least one contact;

at least one solder ball extending between said at least one first substrate first surface contact and said at least one second substrate first surface contact, wherein said at least one solder ball is attached to one of said at least one first substrate first surface contact and said at least one second substrate first surface contact; and

a support structure for imparting pressure between said first substrate and said second substrate.

13. The microelectronic component assembly of claim 12, wherein said support structure comprises:

a frame surrounding a portion of said first substrate,

a backing plate abutting said second substrate second surface;

a thermal plate extending over said frame and adjacent said first substrate second surface; and

a plurality of retention devices extending through said backing plate, said frame, and said thermal plate.

14. The microelectronic component assembly of claim 13, wherein said plurality of retention device comprise a plurality of bolts having at least one nut retaining each of said plurality of bolts.

15. The microelectronic component assembly of claim 12, wherein said first substrate comprises a microelectronic device package including a microelectronic device attached to and in electrical contact with a first surface of an interposer substrate, and wherein said at least first substrate first surface contact comprises at least one contact on a second surface of said interposer substrate.

16. The microelectronic component assembly of claim 15, wherein said support frame comprises

a frame surrounding a portion of said first substrate,

a backing plate abutting said second substrate second surface;

a thermal plate extending over said frame and adjacent said first substrate second surface;

a plurality of retention devices extending through said backing plate, said frame; and the thermal plate; and

a resilient spacer extending between said thermal plate and said interposer substrate.

17. A method of fabricating a microelectronic component assembly, comprising:

providing a first substrate having a first surface and a second surface, wherein said first substrate first surface includes at least one contact;

providing a second substrate having a first surface and a second surface; wherein said second substrate first surface includes at least one contact;

attaching at least one solder ball to one of said at least one first substrate first surface contact and said at least one second substrate first surface contact

aligning said at least one first substrate first surface contact with said at least one second substrate first surface contact; and

imparting pressure between said first substrate and said second substrate with a support structure.

18. A method of fabricating a microelectronic component assembly, comprising:

providing a substrate having at least one contact on a first surface;

disposing a frame on a first surface of a carrier substrate, wherein said carrier substrate first includes at least one contact;

disposing a backing plate on a second surface of said carrier substrate;

inserting a retention device through said backing plate, said carrier substrate, and said frame;

attaching at least one solder ball to one of said at least one contact on said carrier substrate first surface contact and said at least one substrate first surface;

inserting a substrate into said frame, wherein said at least one substrate first surface contact are aligned with said at least one carrier substrate first surface contact;

aligning said at least one first substrate first surface contact with said at least one second substrate first surface contact;

placing a thermal plate is placed over said frame to be retained by said retention device; and

adjusting said retention device to imparting pressure between said substrate and said carrier substrate.

19. The method of claim 18, wherein inserting said retention device comprises inserting at least one bolt and wherein adjusting said retention device comprises adjusting at least one nut on said at least one bolt.

20. The method of claim 18, wherein providing said substrate comprises providing a microelectronic device package including a microelectronic device attached to and in electrical contact with a first surface of an interposer substrate, and wherein said at least one substrate first surface contact comprises at least one contact on a second surface of said interposer substrate.

21. The method of claim 20, further including disposing a thermal interface between a back surface of said microelectronic device and said thermal plate.

22. The method of claim 20, further including disposing a resilient spacer between said interposer substrate and said thermal plate.

23. A substrate contact for forming a non-reflow electrical contact with a solder ball, comprising:

a recess define in a substrate by at least one surface extending into said substrate; and

a conductive material layered in said recess.

24. The substrate contact of claim 23, wherein said surface comprises at least one substantially vertical sidewall.

25. The substrate contact of claim 24, further including a width of said recess, including said layered conductive material, which is substantially the same as a diameter of said solder ball.

25. The substrate contact of claim 23, wherein said at least one surface extending into said substrate comprises a semispherical recess, wherein an upper surface of said conductive material has substantially the same radius as a radius of said solder ball.

26. The substrate contact of claim 25, further including a resilient material disposed between said substrate and said conductive material layer.

27. A substrate contact for forming a non-reflow electrical contact with a solder ball, comprising:

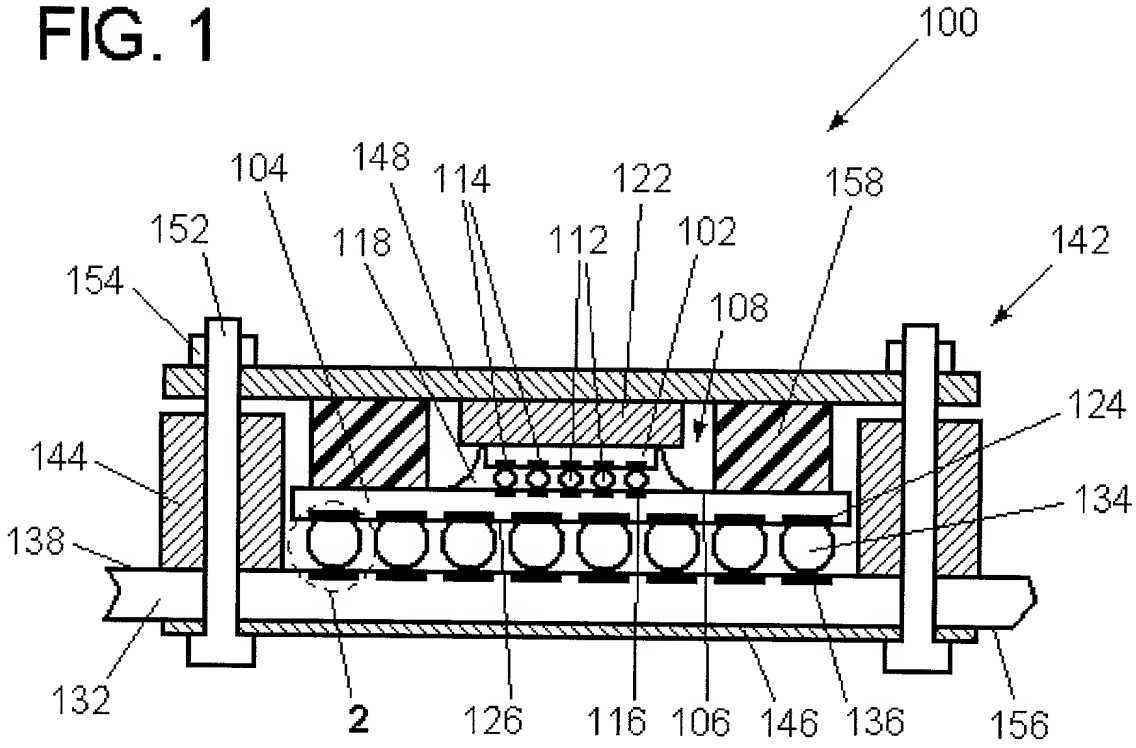
a recess define in a substrate by at least one surface extending into said substrate; and

a conductive material layered over said recess forming a void in said recess.

ABSTRACT OF DISCLOSURE

A surface mount-type microelectronic component assembly which does not physically attach the microelectronic component to its carrier substrate. Electrical contact is achieved between the microelectronic component and the carrier with solder balls attached to either the microelectronic component or the carrier substrate. A force is exerted on the assembly to achieve sufficient electrical contact between the microelectronic component and the carrier substrate.

FIG. 1


100
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156

FIG. 2a

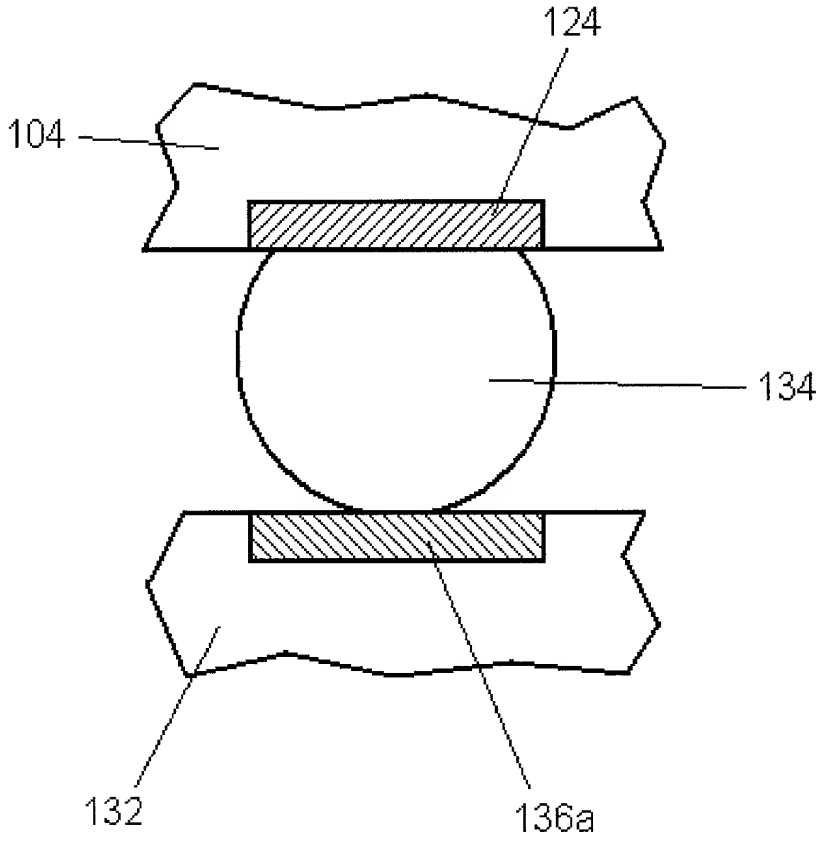


FIG. 2b

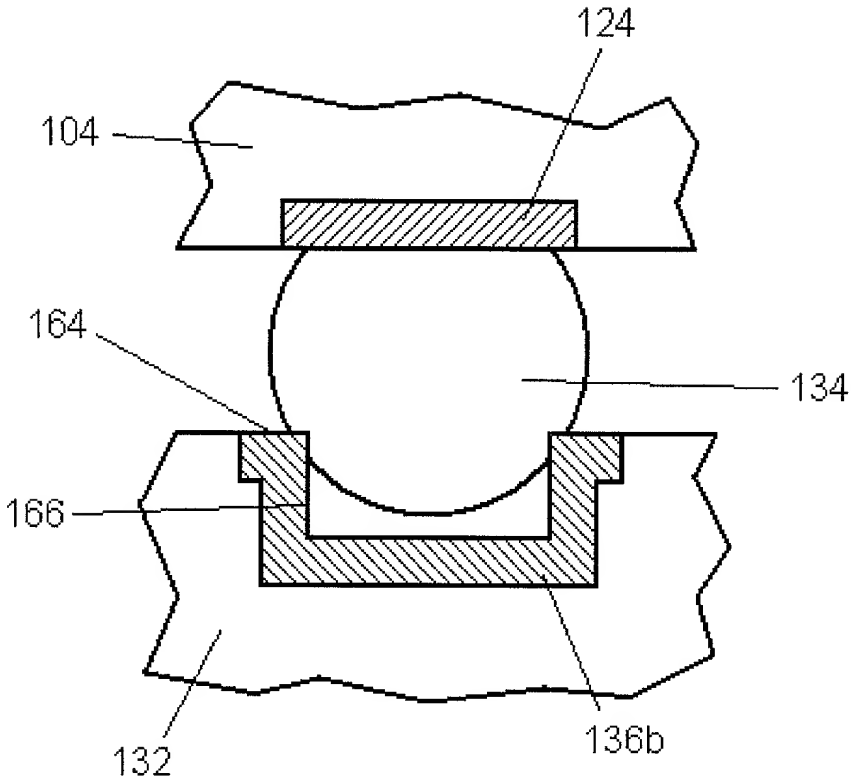


FIG. 2c

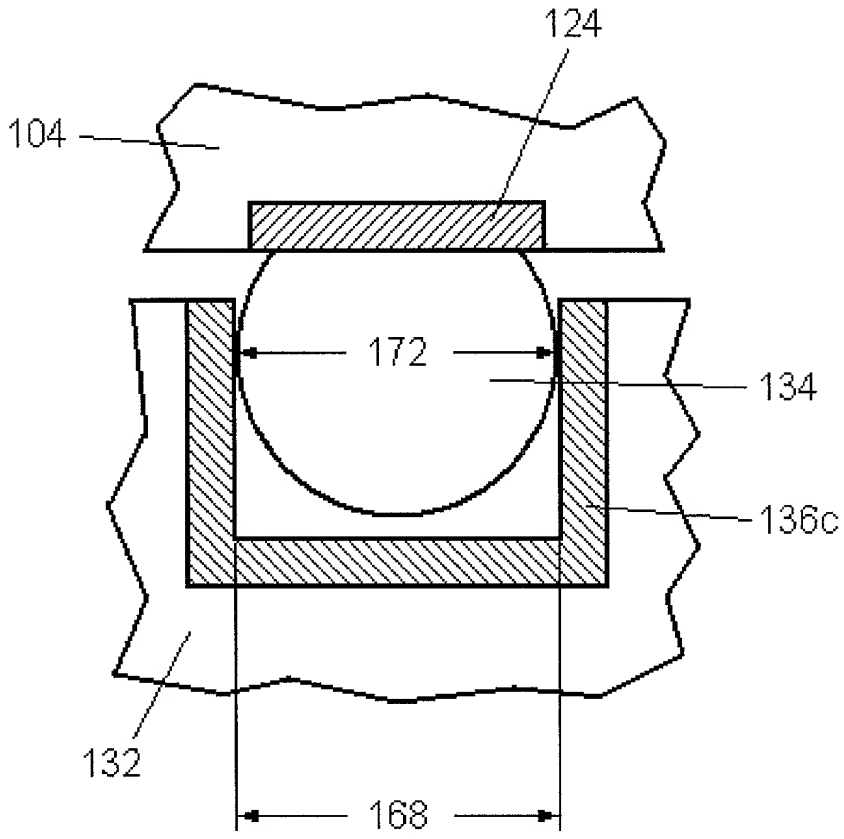


FIG. 2d

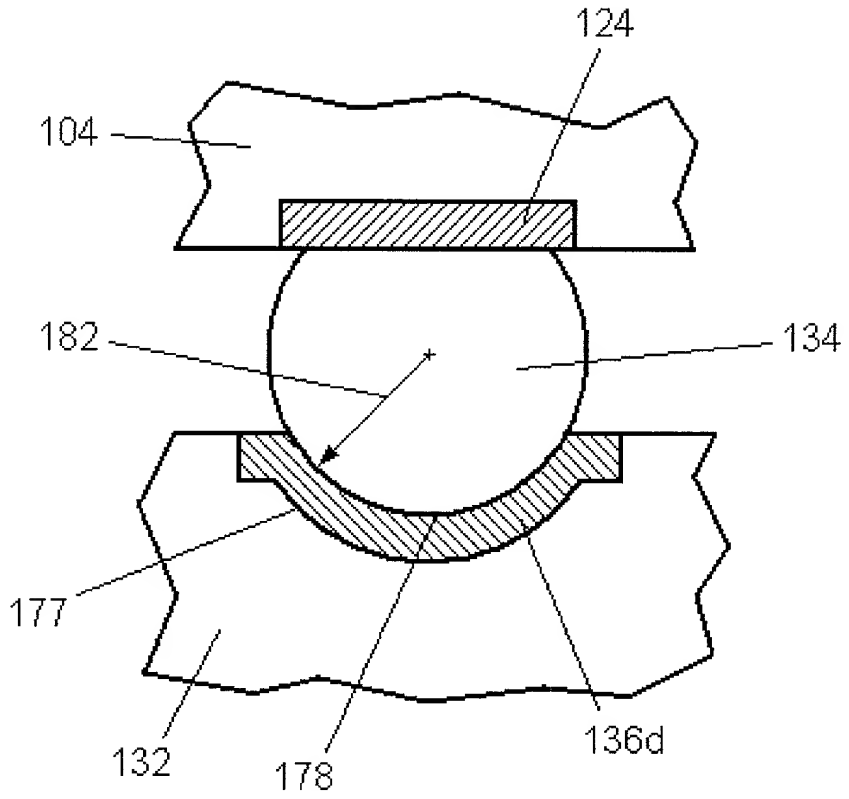


FIG. 2e

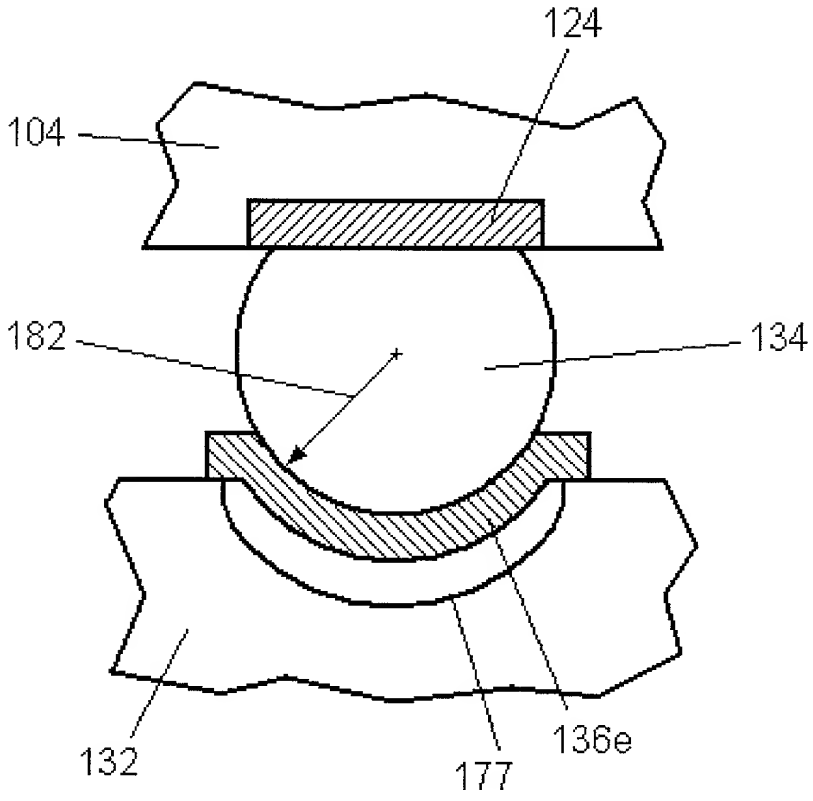


FIG. 2f

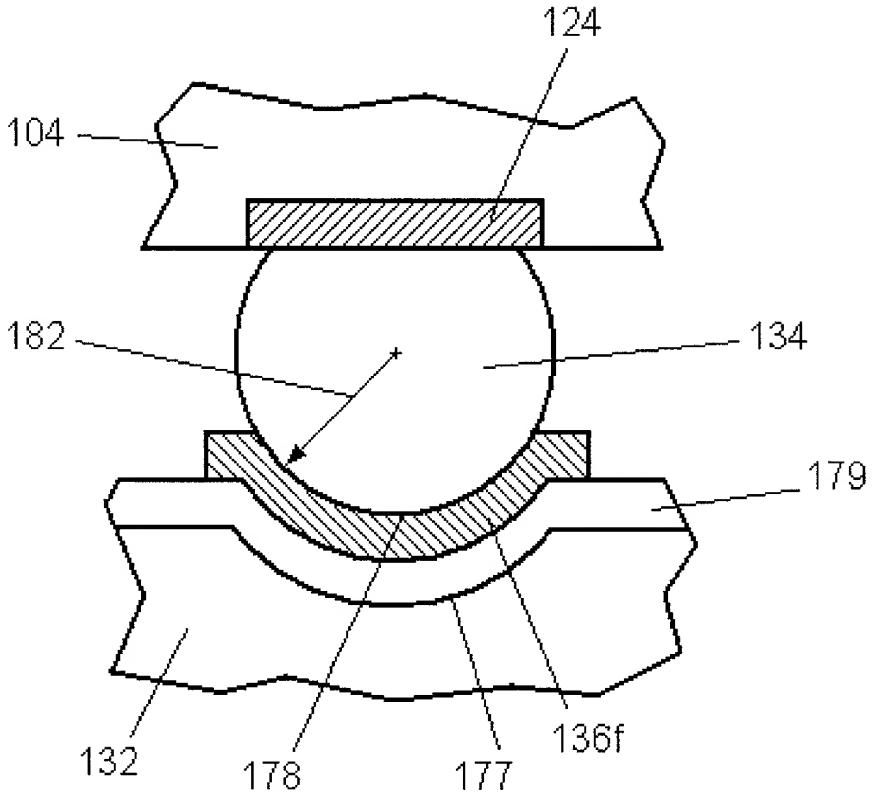


FIG. 2g

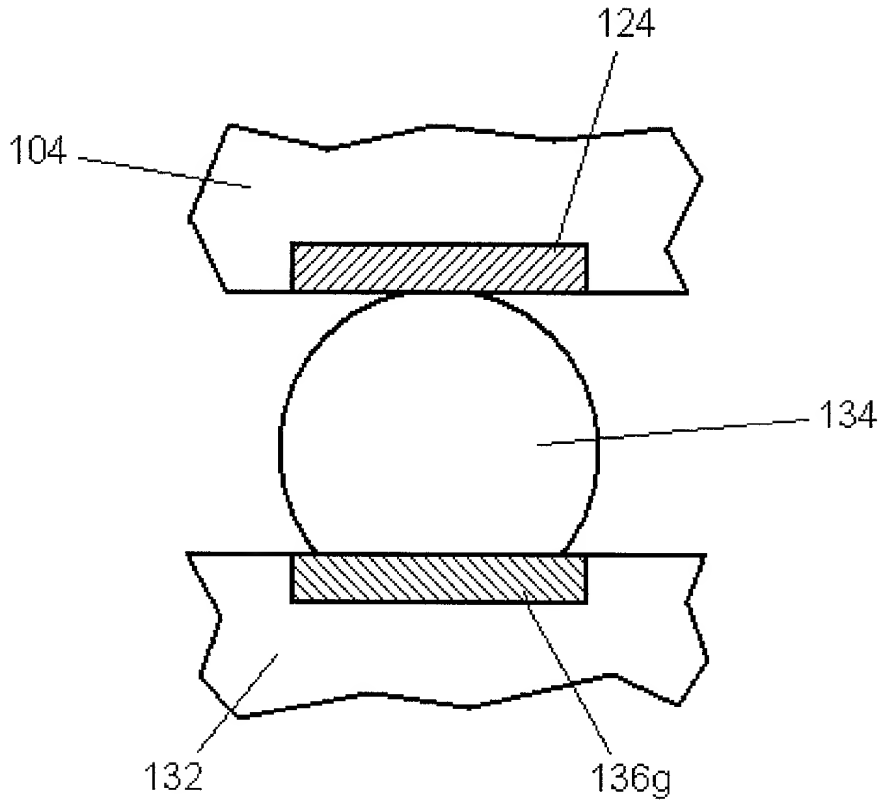


FIG. 3

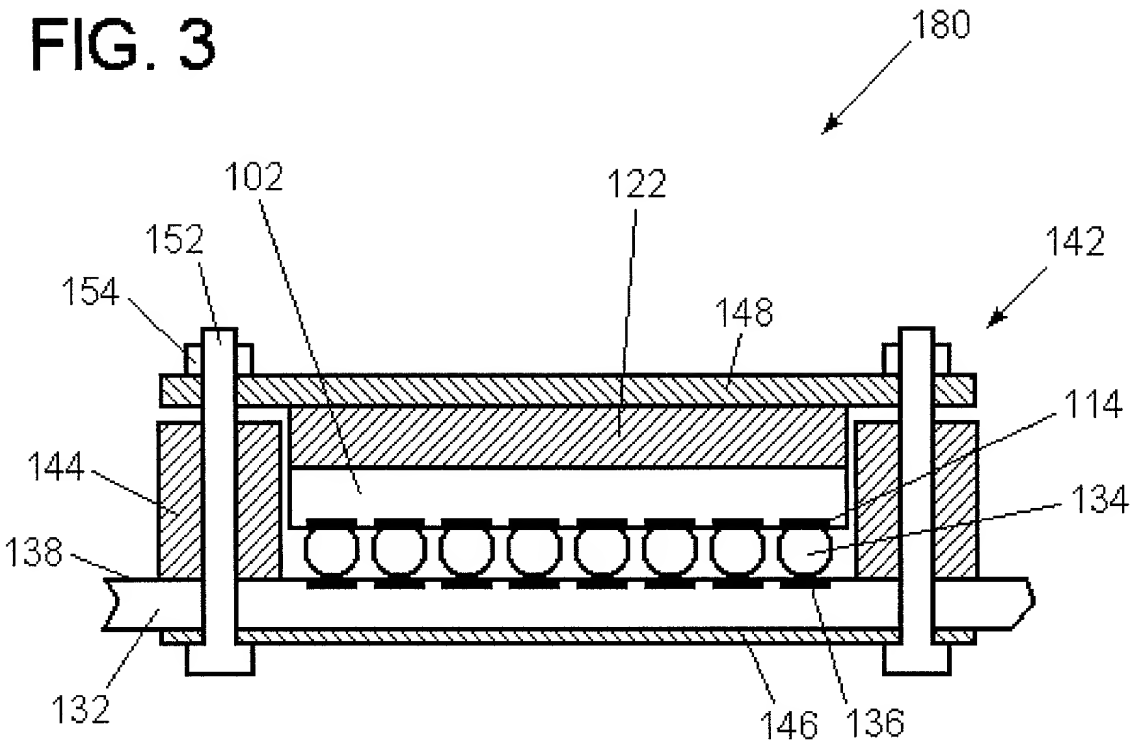


FIG. 4

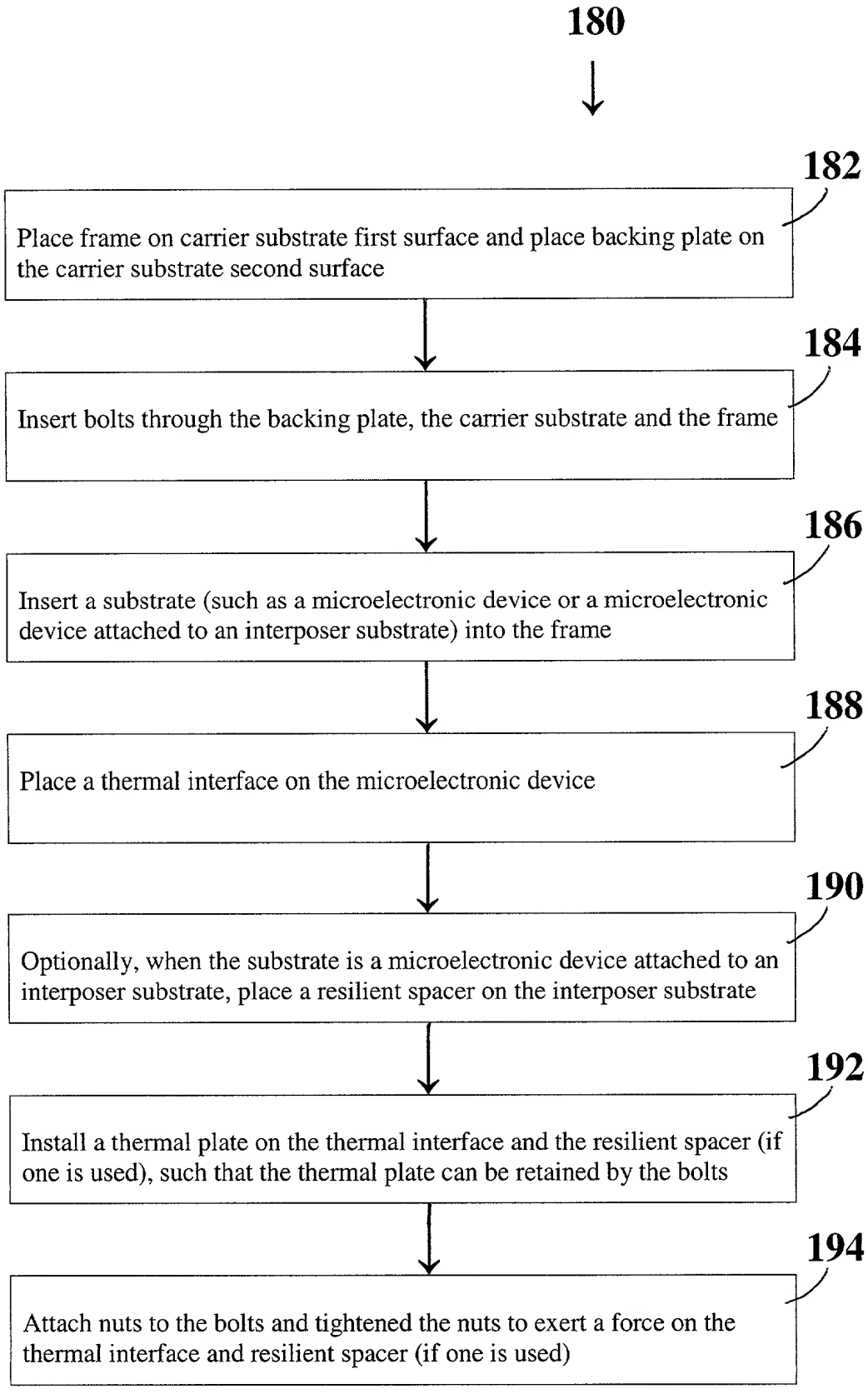
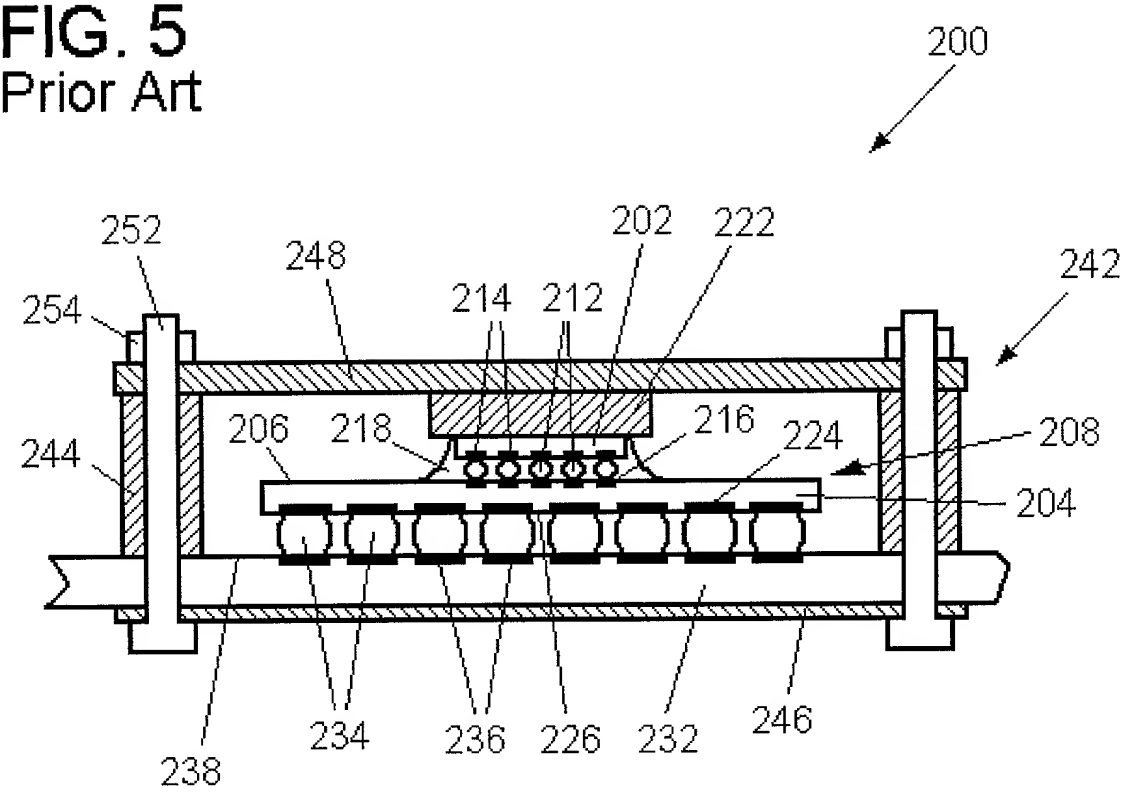

180
182
Place frame on carrier substrate first surface and place backing plate on the carrier substrate second surface
184
Insert bolts through the backing plate, the carrier substrate and the frame
186
Insert a substrate (such as a microelectronic device or a microelectronic device attached to an interposer substrate) into the frame
188
Place a thermal interface on the microelectronic device
190
Optionally, when the substrate is a microelectronic device attached to an interposer substrate, place a resilient spacer on the interposer substrate
192
Install a thermal plate on the thermal interface and the resilient spacer (if one is used), such that the thermal plate can be retained by the bolts
194
Attach nuts to the bolts and tightened the nuts to exert a force on the thermal interface and resilient spacer (if one is used)

FIG. 5
Prior Art



Attorney's Docket No.: 42390.P7663 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

DIRECT BGA ATTACHMENT WITHOUT SOLDER REFLOW

the specification of which

XX is attached hereto.
___ was filed on _____ as
United States Application Number _____
or PCT International Application Number_____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status -- patented, pending, abandoned
Application Number	Filing Date	Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Robert G. Winkle, Intel Corporation, BLAKELY, SOKOLOFF, TAYLOR &
(Name of Attorney or Agent)
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(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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